
LIONIX
INTERNATIONAL
Our chips drive your business
www.lionix-international.com

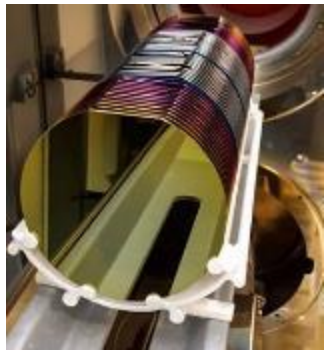
Who we are

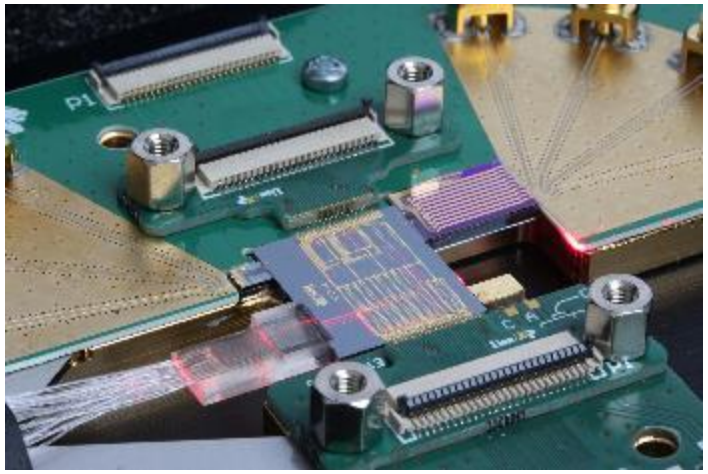
- Located in the Netherlands
- Established in 2001 (LioniX)
- ~60 employees
- Production location in
  - Enschede, Netherlands
    - LioniX International Labs
    - Assembly facilities
    - Nanolab cleanroom

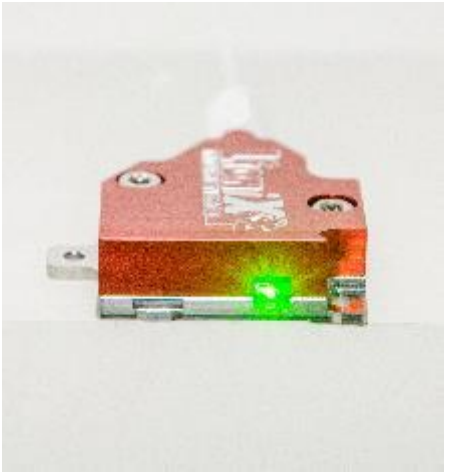
Know-how phase | **Demonstration phase** | **Optimization phase** | **Stabilization phase** | **Realization phase** | **Production phase**

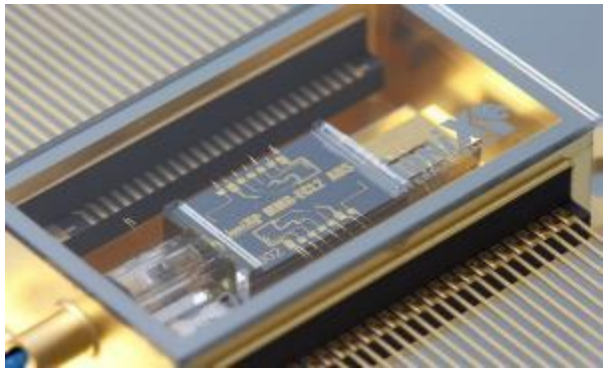
Strategy

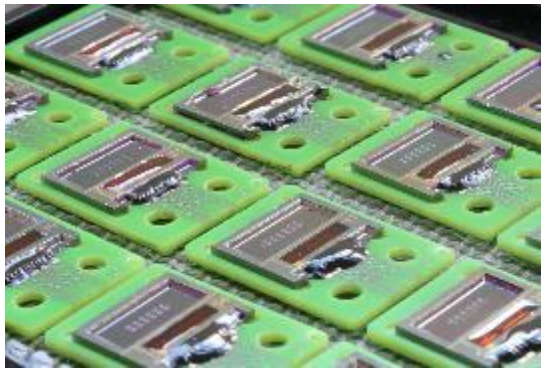
- Make custom devices for different applications, from telecommunications to healthcare
- Help customers all the way from design to device, in complete modules, at their desired volumes
- Patent our technology to protect our tricks, let them patent their devices to protect their products







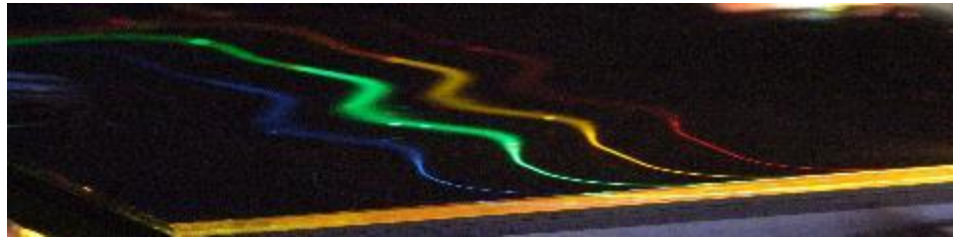




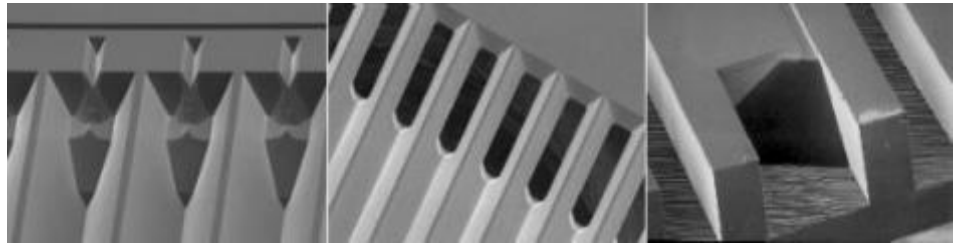
What We Do

Customized Microsystem Solutions

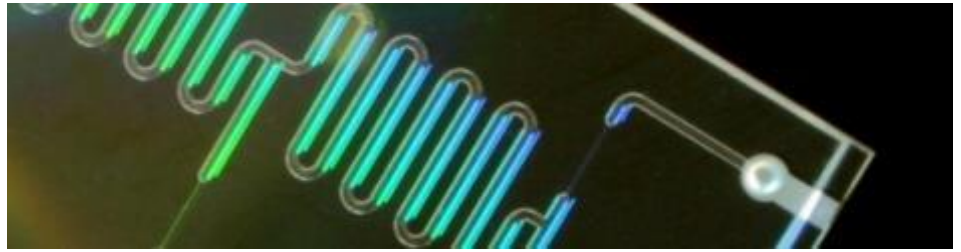
Integrated Photonics



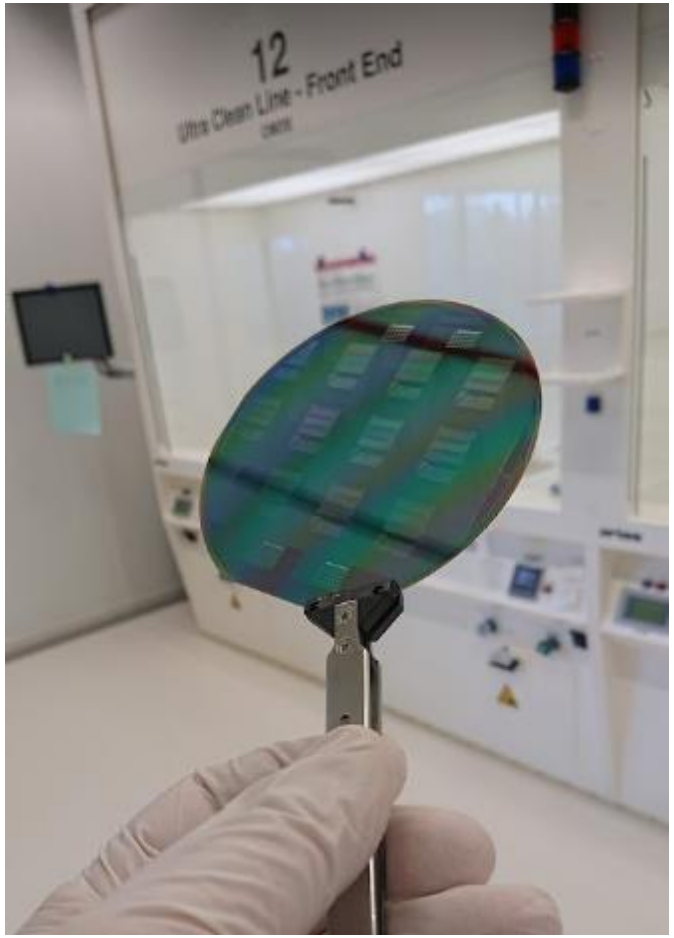
Customized MEMS

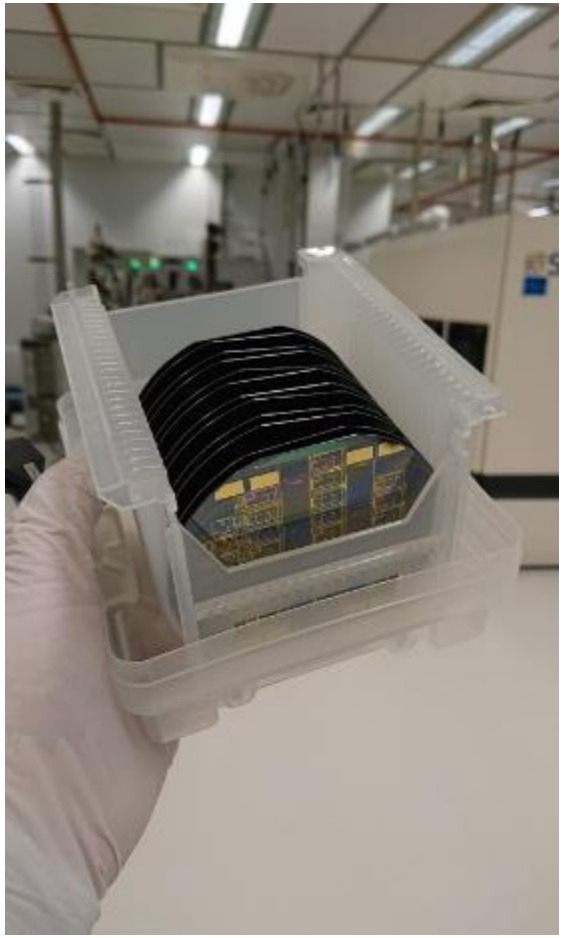


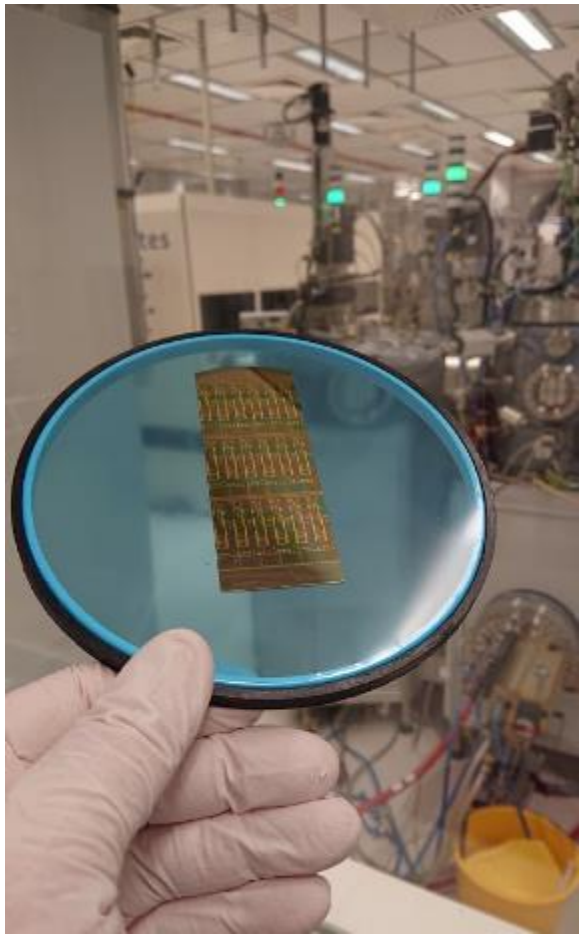
(Opto) Fluidics

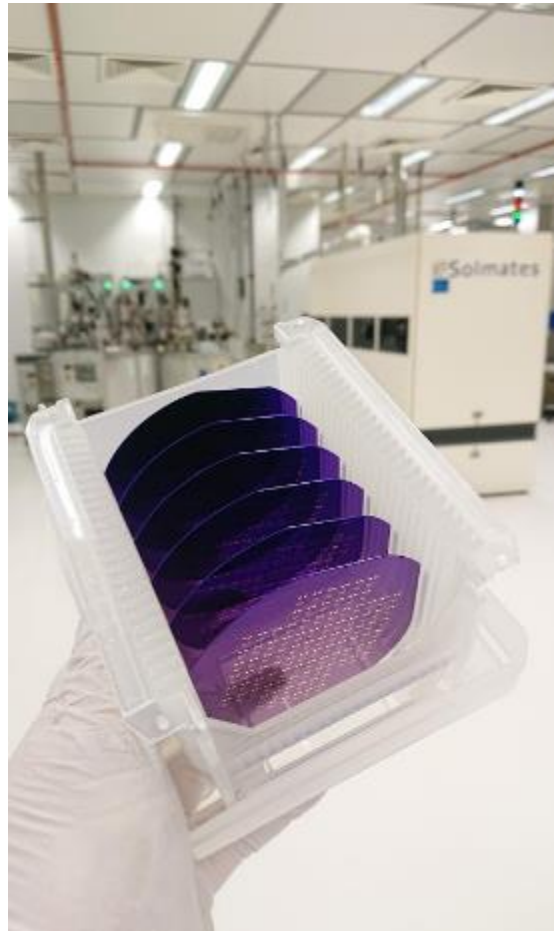


Chip fabrication



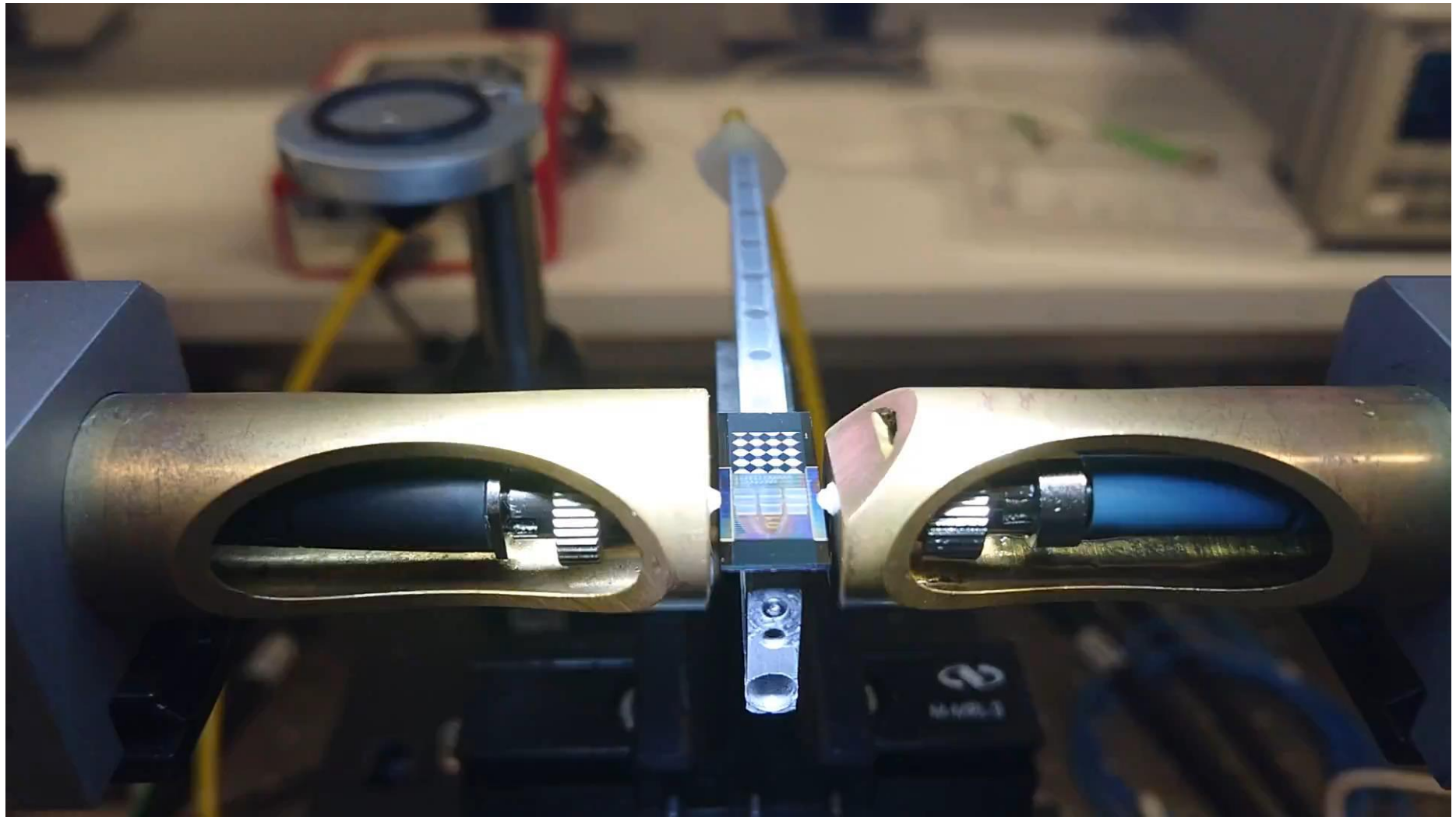




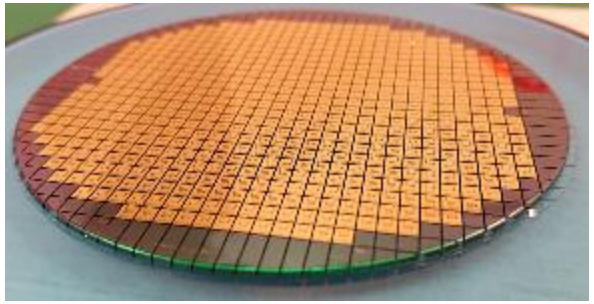


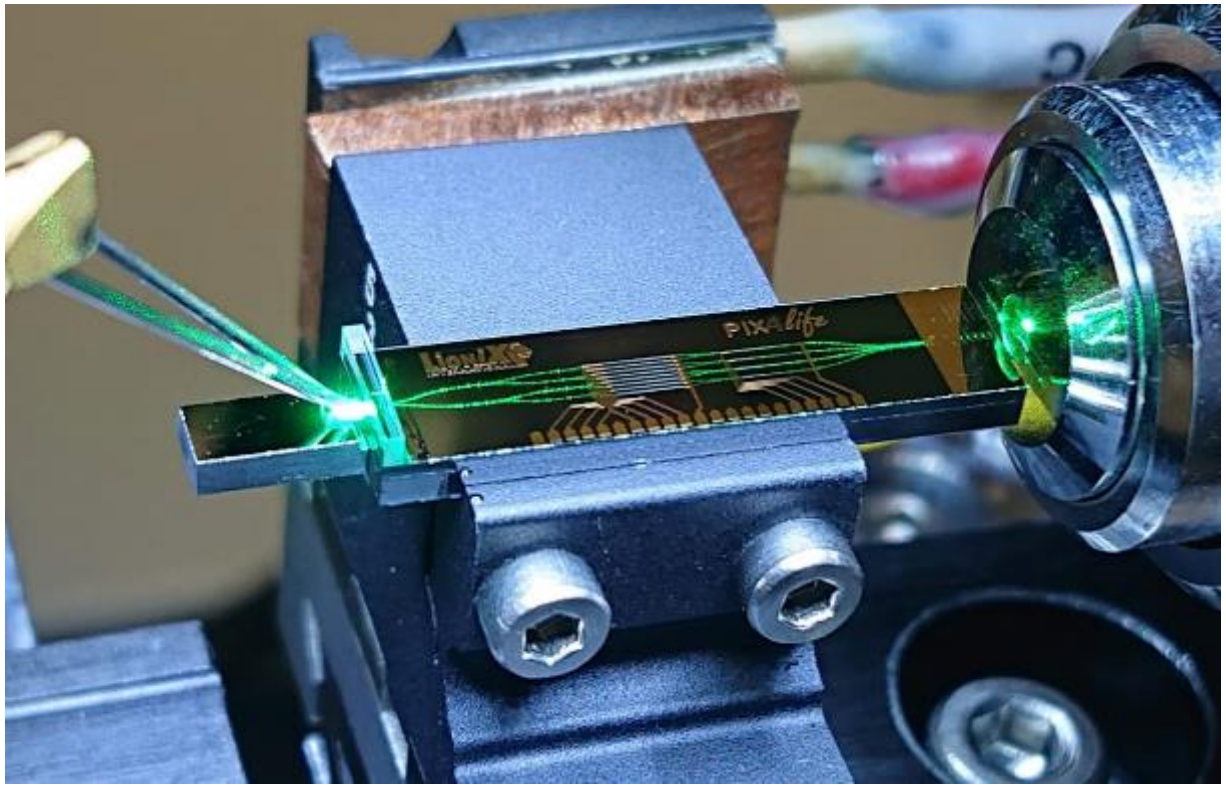
Nanolab

Chip Testing



Module Assembly





Tasks of a Project Leader

- Ivo Hegeman
- Project Leader and Design Engineer
- Studied physics at UT
- Graduated at OS group (these days IOS group)
- Couple years at UT
- At LioniX for 2 years now

Ivo Hegeman • 2nd
Project leider bij LioniX International
Enschede

Tasks of a Project Leader

Main task: making sure customers get what they need, everything from A to Z.

- Meetings with customers
- Translate requirements into technical aspects
- Preparing functional designs, cleanroom processes, lithography masks etc.
- Lots of communication
- Some paperwork ☹

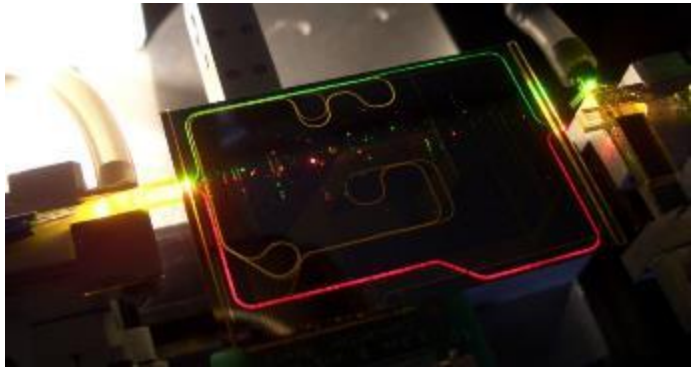
Also some technical side tasks:

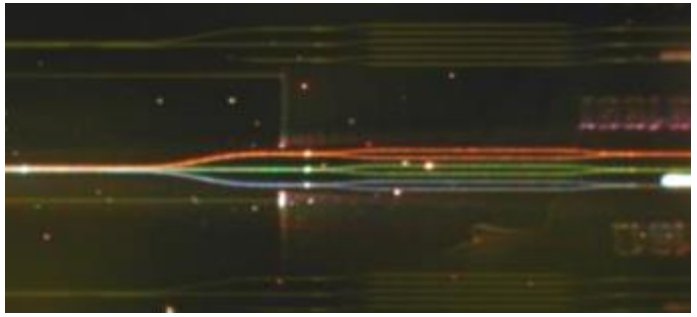
- Some cleanroom work
- Assembly of (simple) modules
- Characterization work
- Anything else that passes by and I like to pick up

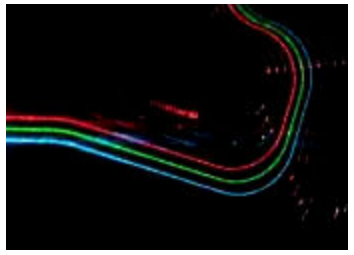
What is a PIC?

Photonic Integrated Circuits

- Photonic Integrated Circuits (PICs) integrate several optical functions
- PICs fabricated with a wafer-scale technology on substrates of silicon, silica, or a non-linear crystal material
- PICs use waveguides to allow the realization of
  - Couplers
  - Wavelength filters
  - Power splitters
  - Combiners
  - Active elements with optical gain or attenuation







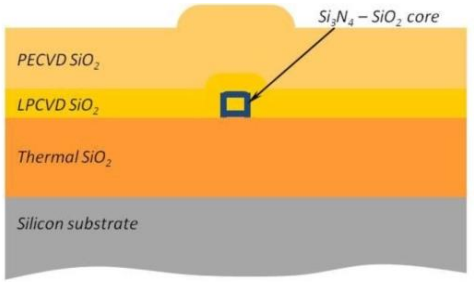
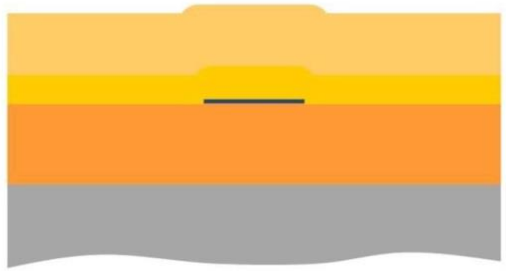
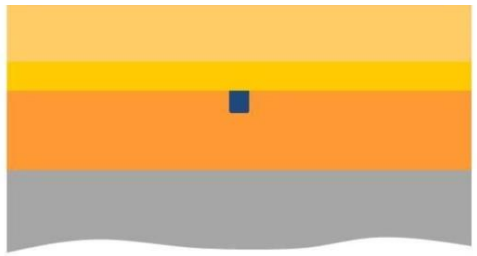
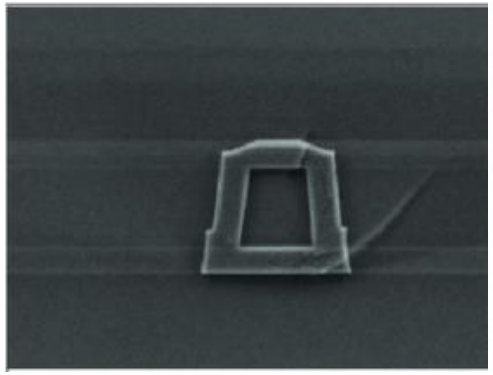
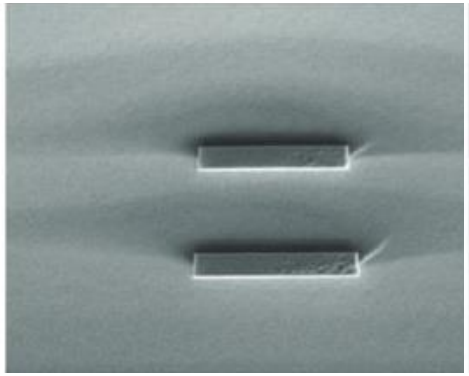
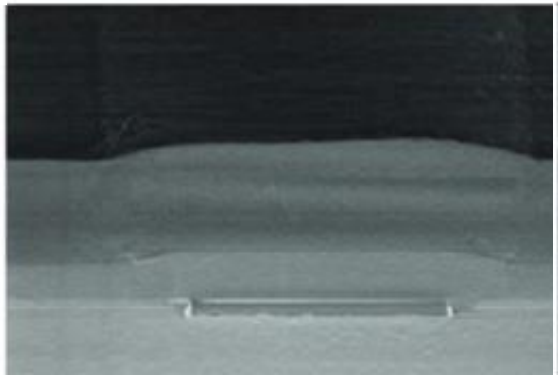
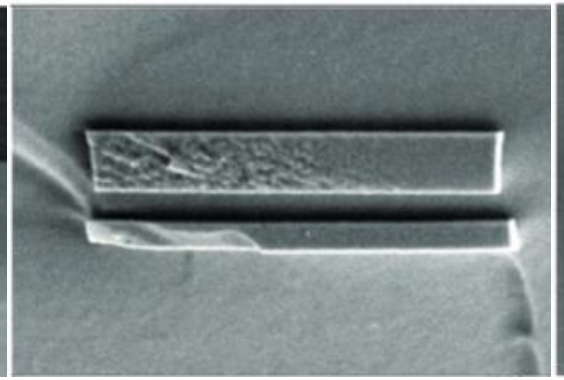
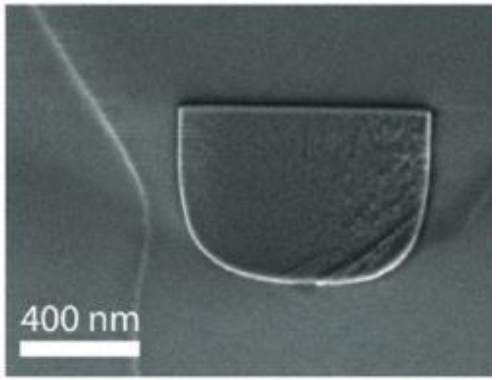
Coupler; x and y fixed; determined by design

Splitter; typically cascade of 50/50 splitter

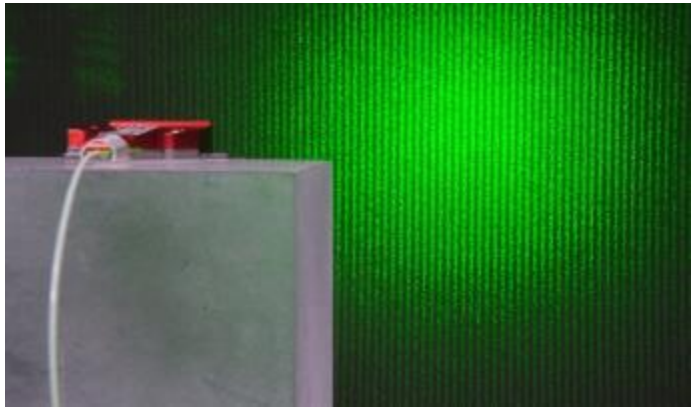
Combiner; typically adding proportionally

Active coupler

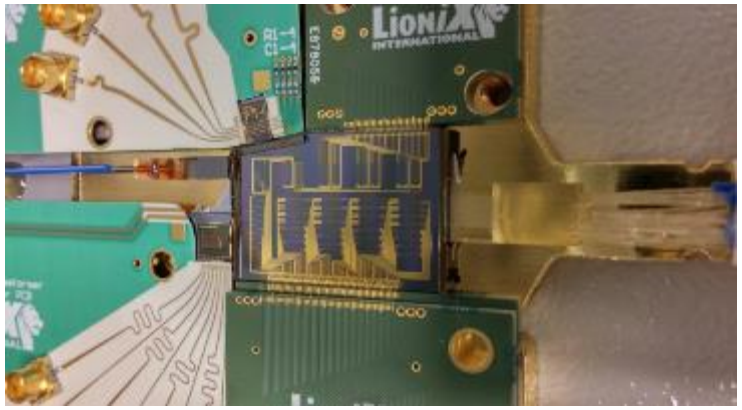
TriPleX® waveguide

Box shell	*Symmetric double stripe*	*Single stripe geometry*	*Asymmetric double stripe*	*Filled box*
				
				
Reduced polarization dependence High and low index contrast variants	Tight bending radii Birefringence at 5.3×10^{-2}	Very low propagation losses Larger bending radii	Spot size conversion feasible, low loss, modest to high confinement	Ultrahigh confinement Minimum bending radius of 12.5µm

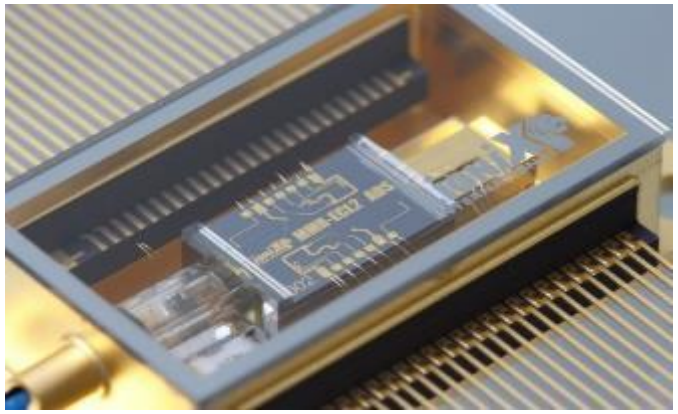
Application examples



DNA sequencing

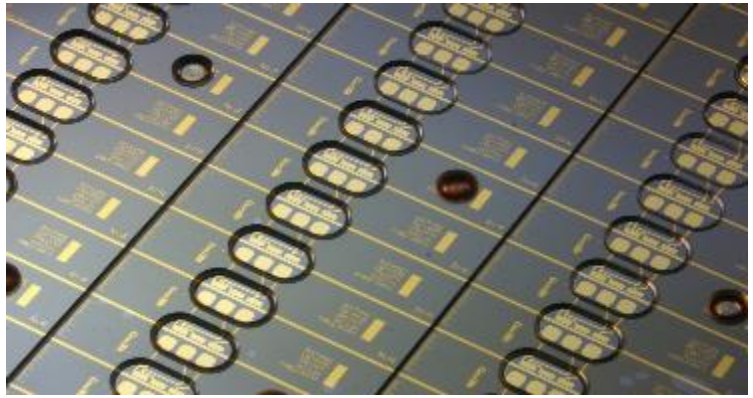


5G antenna systems

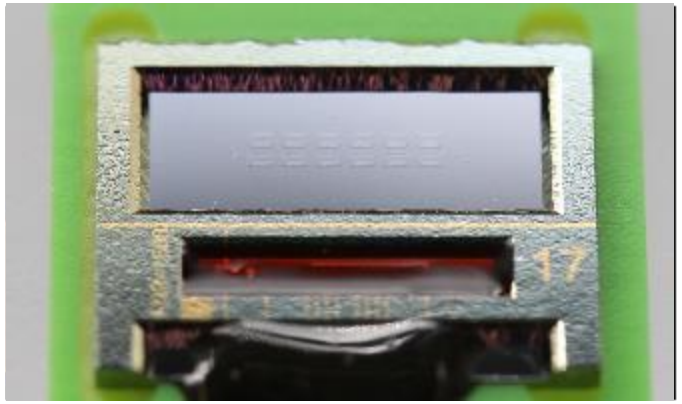


Tunable lasers for sensing and telecom

Compact Light Engines: AR/VR



Medical imaging (OCT)

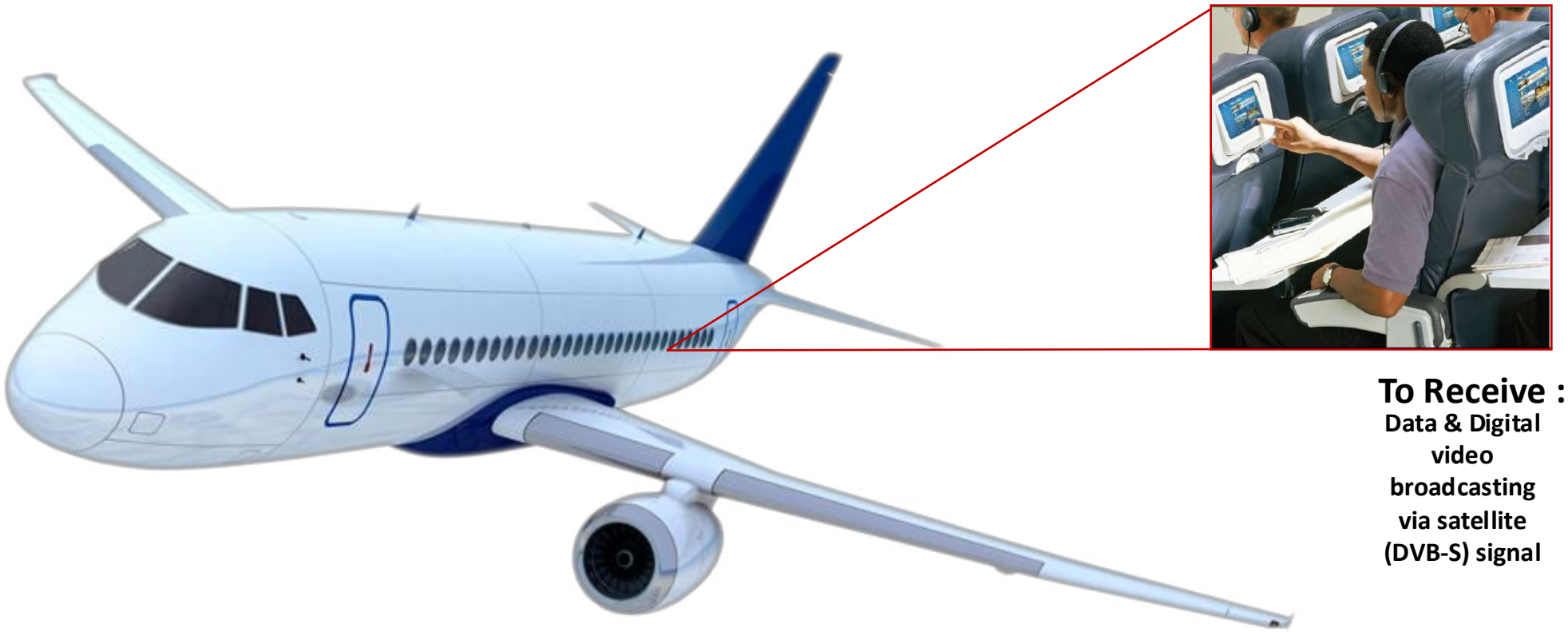


Biosensors

Satellite Communications

A Fully Integrated Example

A Problem Onboard



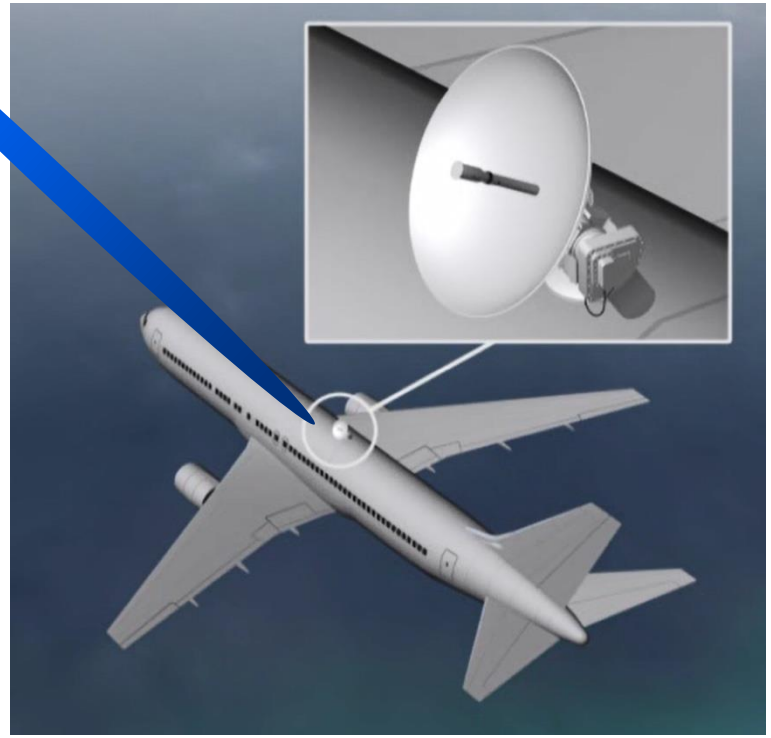
To Receive :

Data & Digital video broadcasting via satellite (DVB-S) signal

A Problem Offboard

Required :

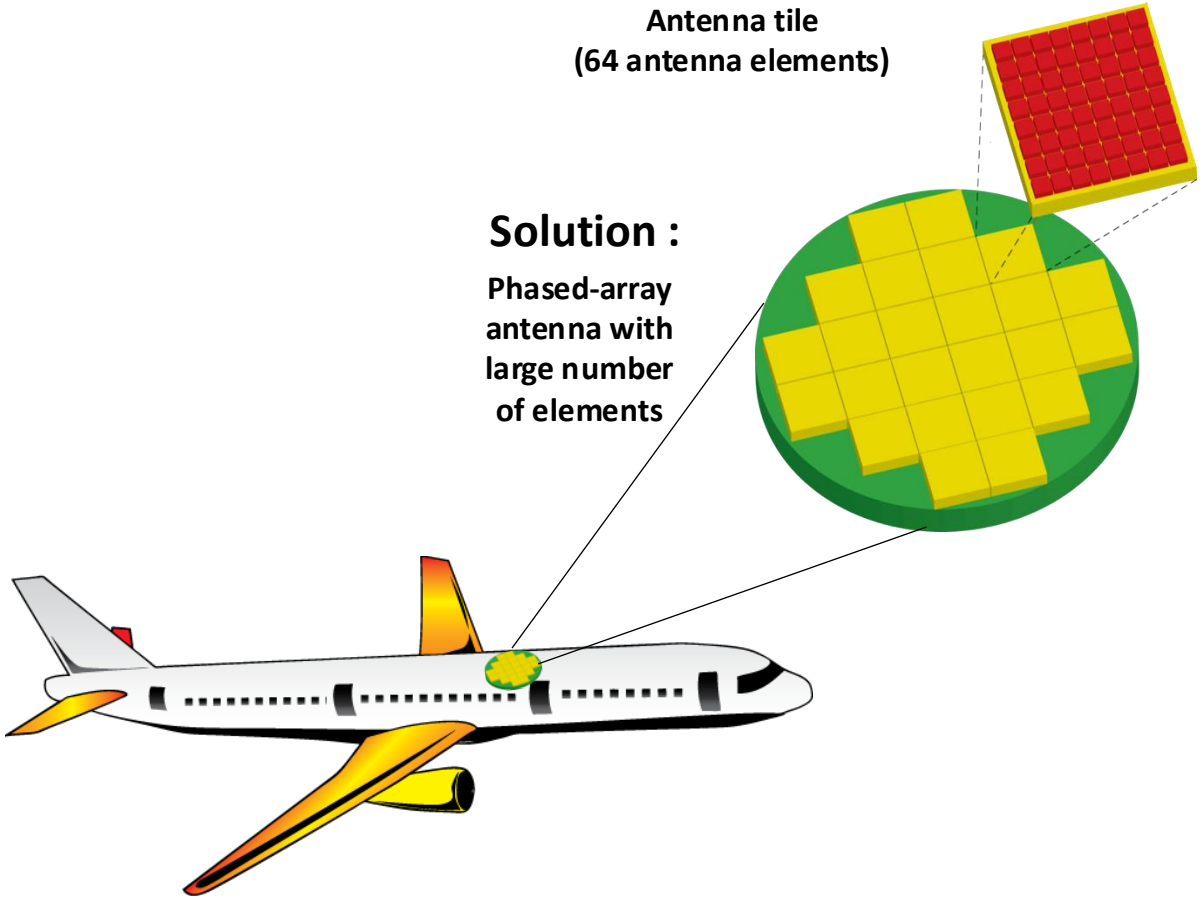
Broadband, continuous and squint-free beamsteering



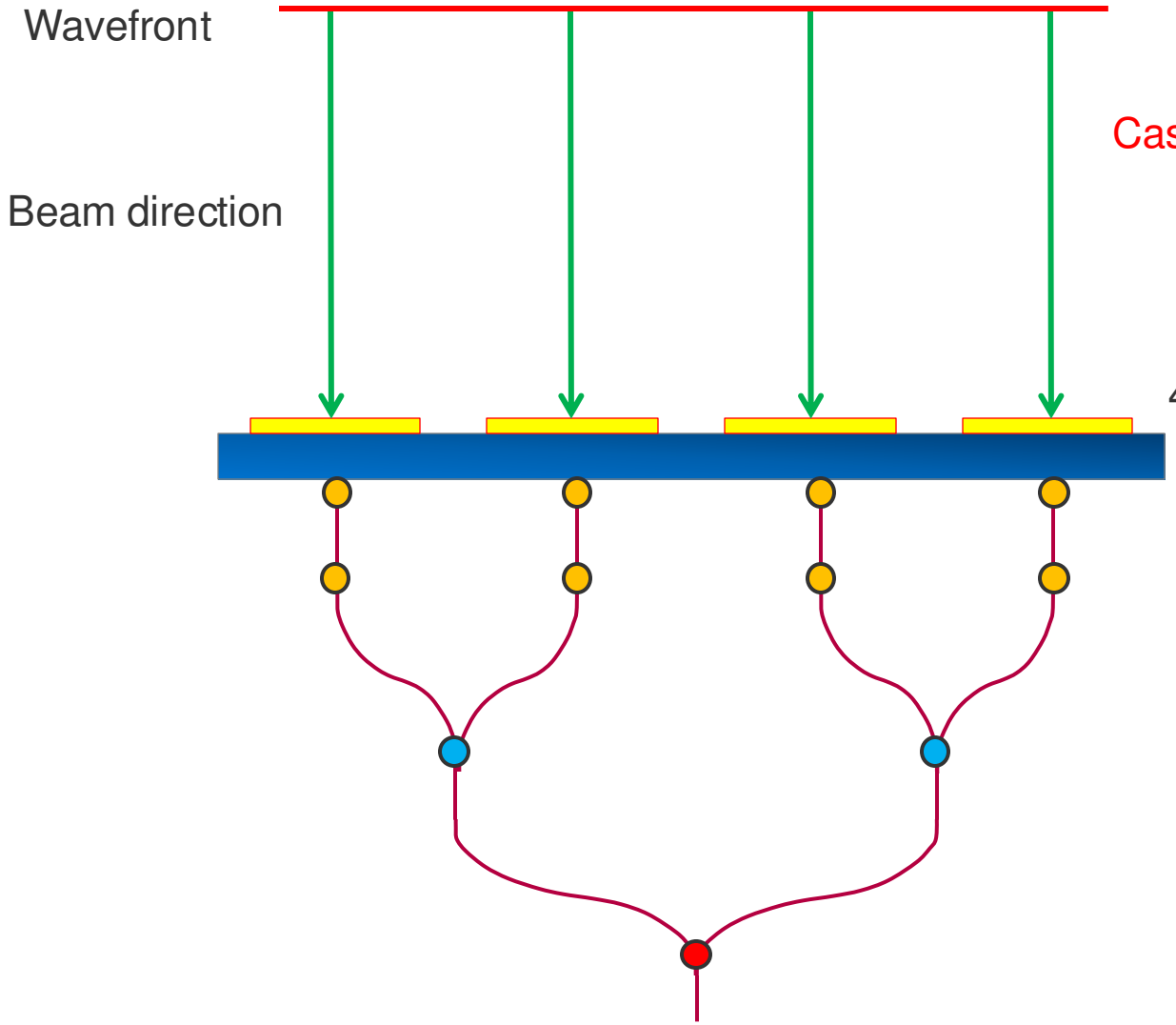
Solution :

Phased-array antenna with large number of elements

Antenna tile (64 antenna elements)

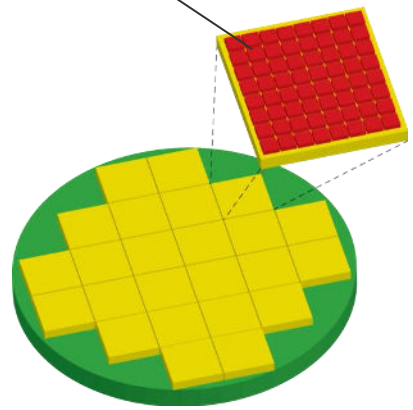


Signal Reception

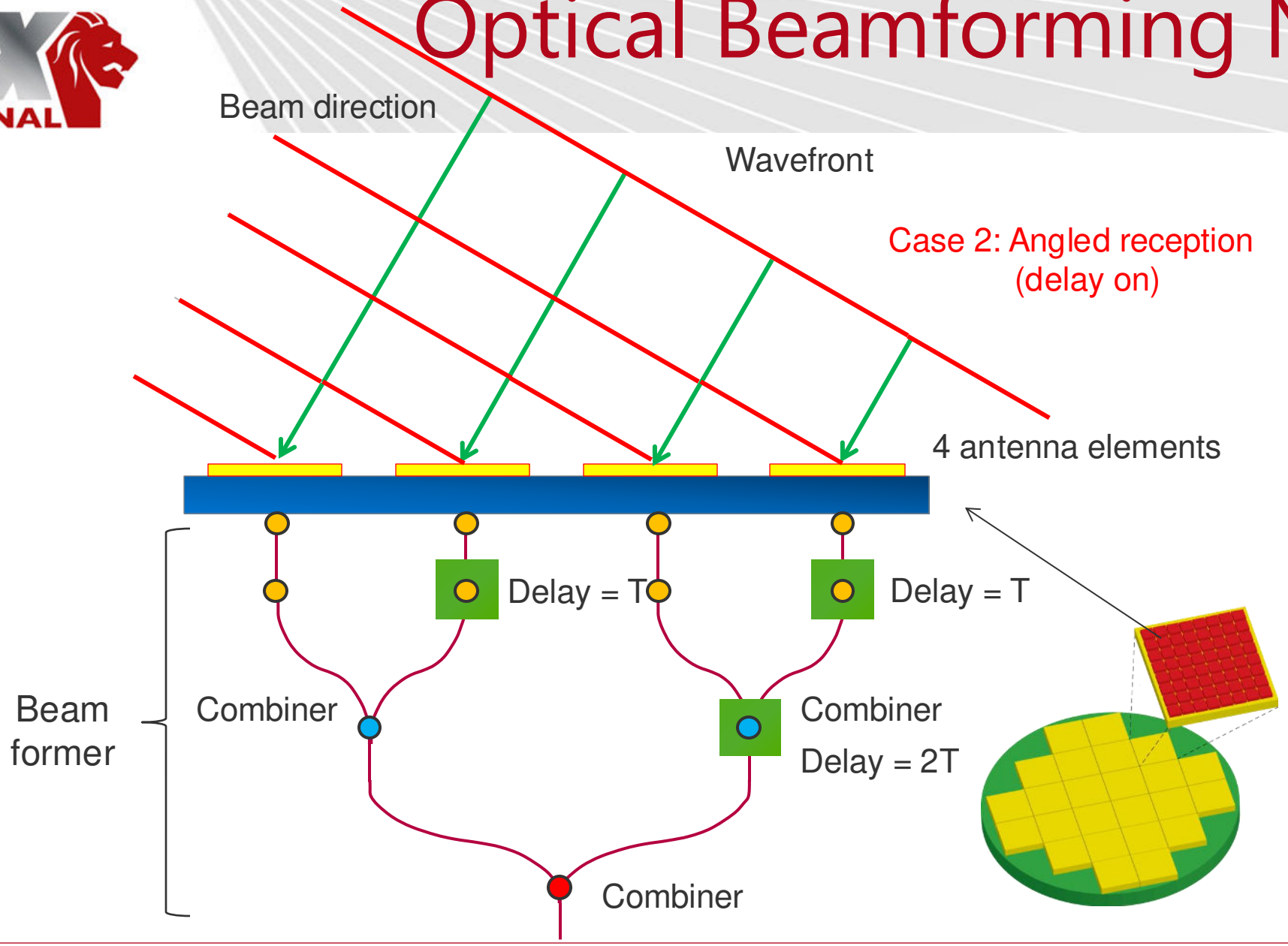


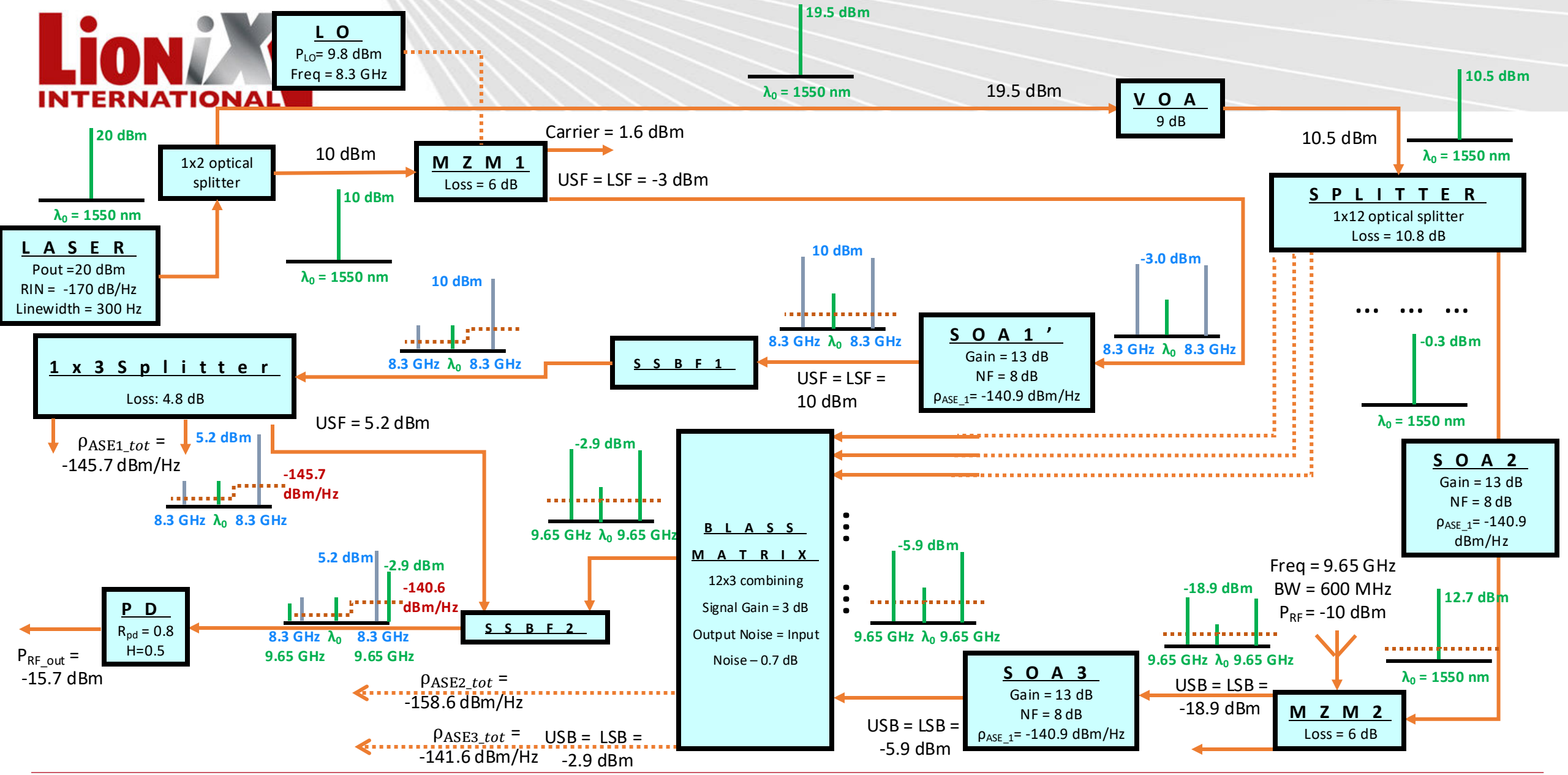
Case 1: Broadside reception

4 antenna elements

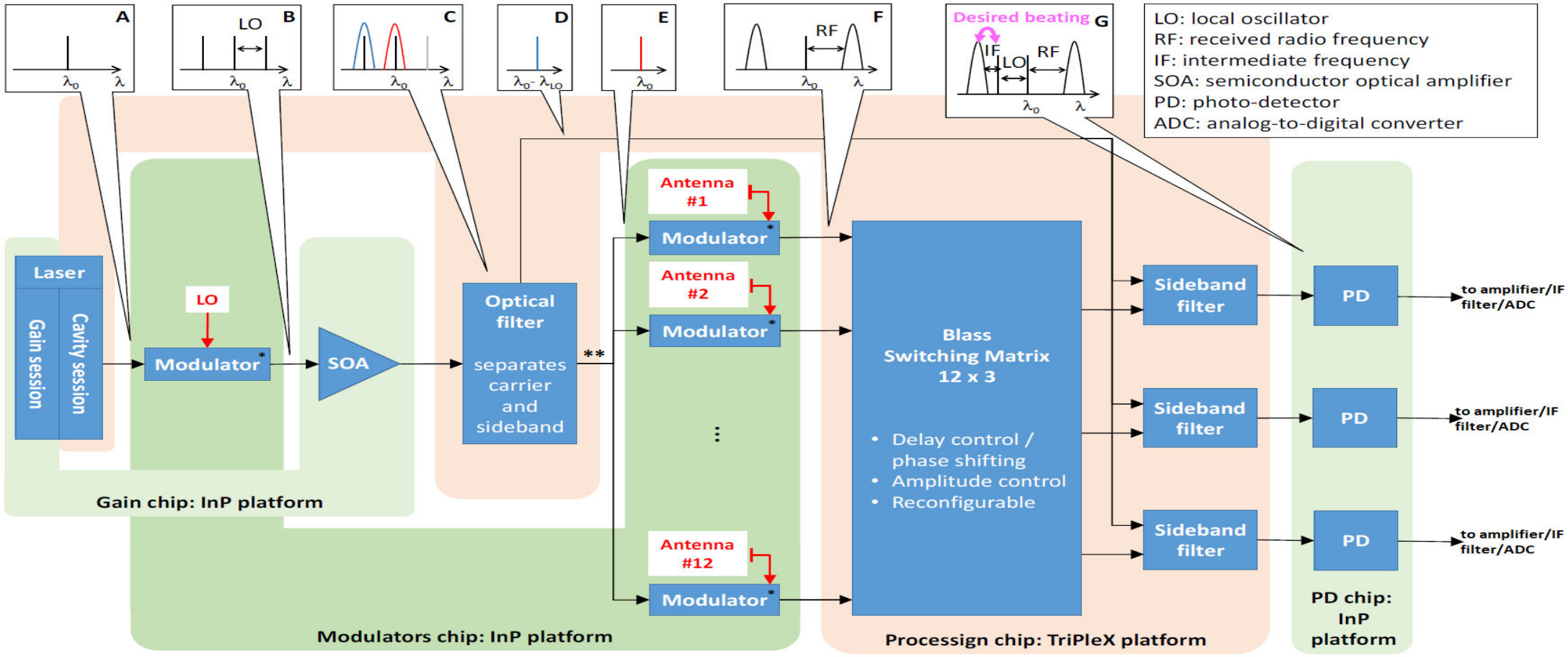


Optical Beamforming Network



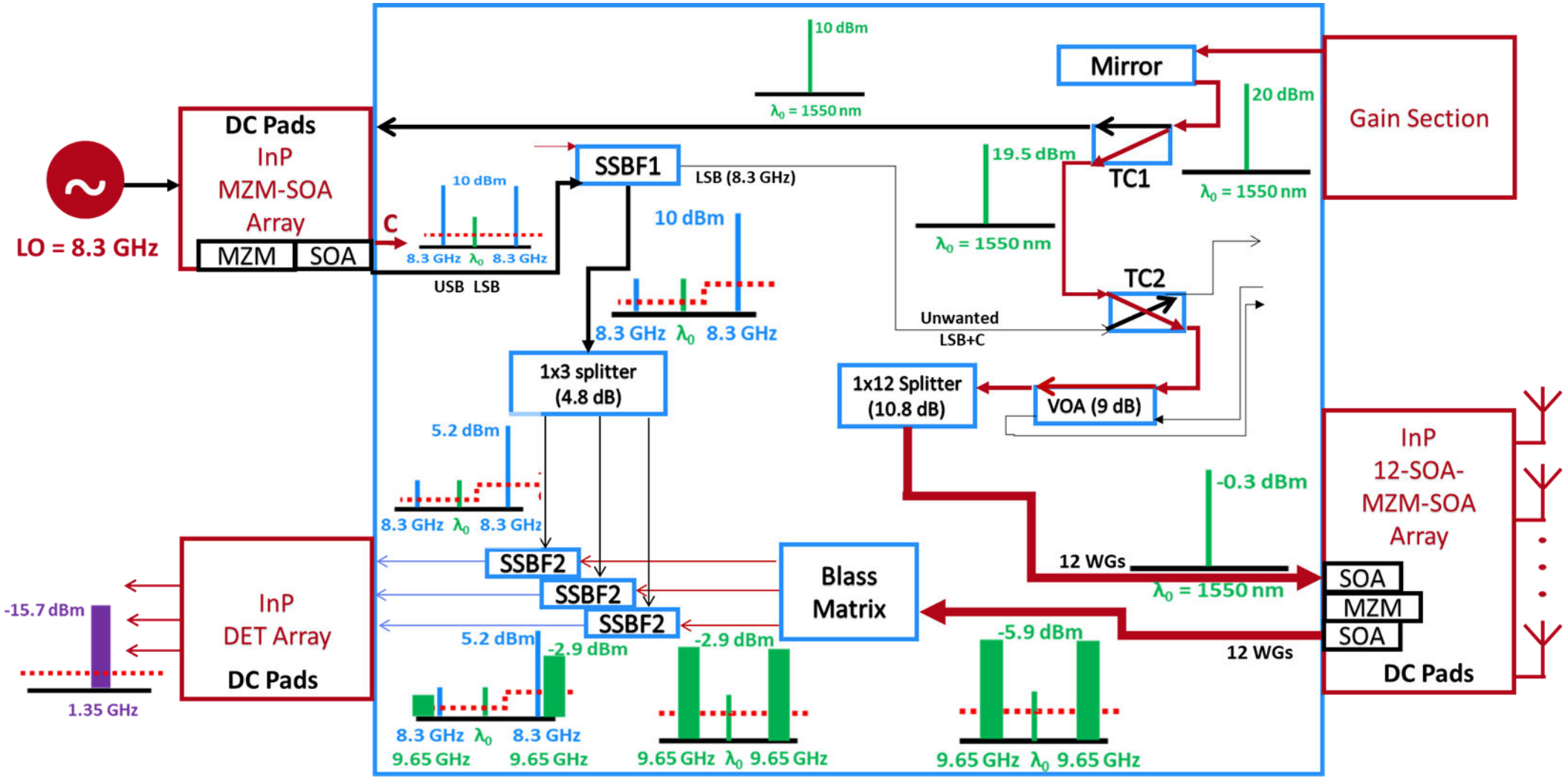

LO
P_{LO}= 9.8 dBm
Freq = 8.3 GHz
19.5 dBm
λ_0 = 1550 nm
19.5 dBm
VOA
9 dB
10.5 dBm
10.5 dBm
λ_0 = 1550 nm
20 dBm
λ_0 = 1550 nm
1x2 optical splitter
10 dBm
MZM 1
Loss = 6 dB
Carrier = 1.6 dBm
USF = LSF = -3 dBm
SPLITTER
1x12 optical splitter
Loss = 10.8 dB
LASER
Pout =20 dBm
RIN = -170 dB/Hz
Linewidth = 300 Hz
10 dBm
λ_0 = 1550 nm
10 dBm
8.3 GHz λ_0 8.3 GHz
10 dBm
8.3 GHz λ_0 8.3 GHz
-3.0 dBm
8.3 GHz λ_0 8.3 GHz
SOA 1'
Gain = 13 dB
NF = 8 dB
ρ_{ASE_1}= -140.9 dBm/Hz
-0.3 dBm
λ_0 = 1550 nm
1 x 3 Splitter
Loss: 4.8 dB
SSBF 1
USF = LSF = 10 dBm
USF = 5.2 dBm
ρ_{ASE1_tot} = -145.7 dBm/Hz
5.2 dBm
-145.7 dBm/Hz
8.3 GHz λ_0 8.3 GHz
-2.9 dBm
9.65 GHz λ_0 9.65 GHz
SOA 2
Gain = 13 dB
NF = 8 dB
ρ_{ASE_1}= -140.9 dBm/Hz
BLASS MATRIX
12x3 combining
Signal Gain = 3 dB
Output Noise = Input Noise – 0.7 dB
-5.9 dBm
9.65 GHz λ_0 9.65 GHz
Freq = 9.65 GHz
BW = 600 MHz
P_{RF} = -10 dBm
-18.9 dBm
9.65 GHz λ_0 9.65 GHz
12.7 dBm
λ_0 = 1550 nm
5.2 dBm
-2.9 dBm
-140.6 dBm/Hz
8.3 GHz λ_0 9.65 GHz
8.3 GHz 9.65 GHz
SSBF 2
PD
R_{pd} = 0.8
H=0.5
P_{RF_out} = -15.7 dBm
ρ_{ASE2_tot} = -158.6 dBm/Hz
ρ_{ASE3_tot} = -141.6 dBm/Hz
USB = LSB = -2.9 dBm
SOA 3
Gain = 13 dB
NF = 8 dB
ρ_{ASE_1}= -140.9 dBm/Hz
USB = LSB = -5.9 dBm
USB = LSB = -18.9 dBm
MZM 2
Loss = 6 dB

Beamformer Architecture

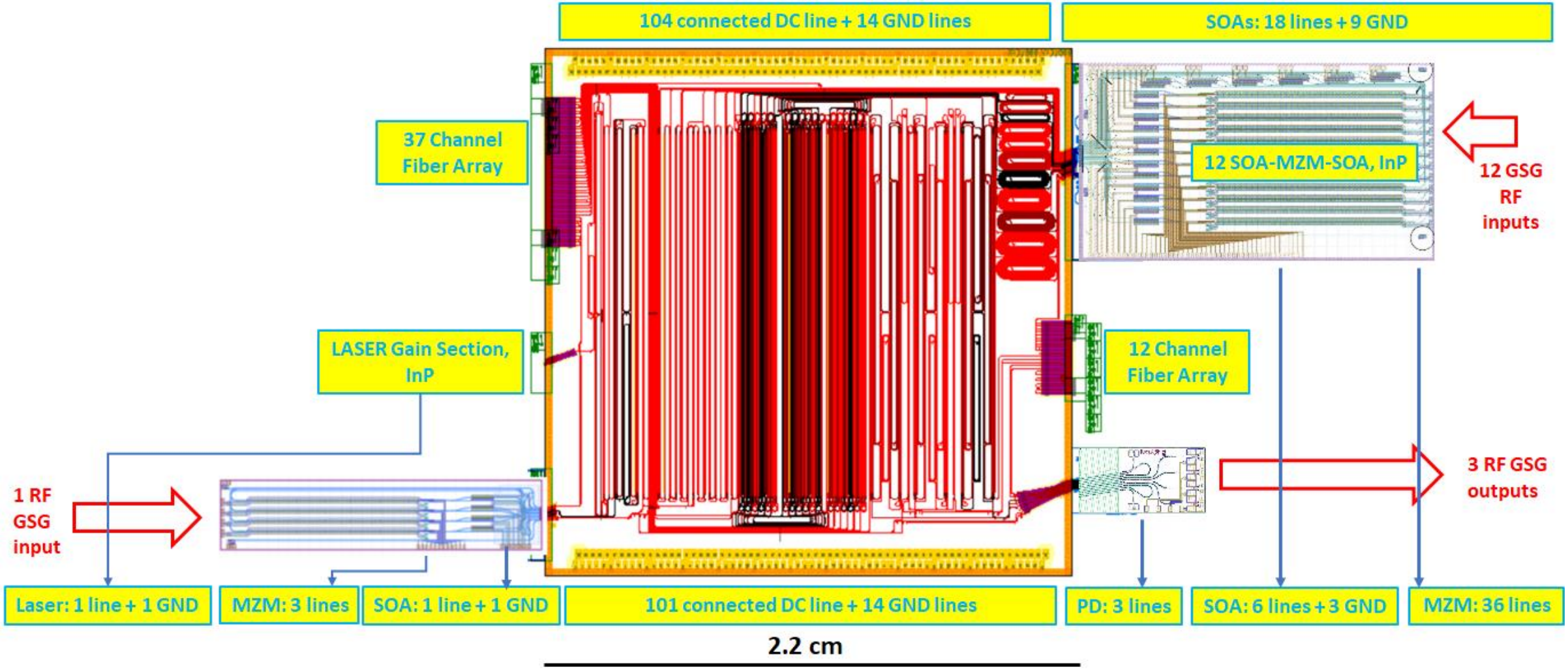


*: Modulator integrated with SOA **: VOA followed by 1x12 splitter

Functional Layout



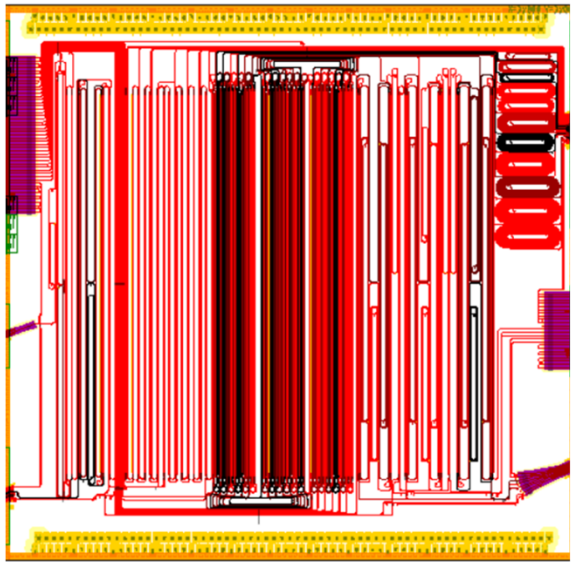
Mask & Assembly Designs



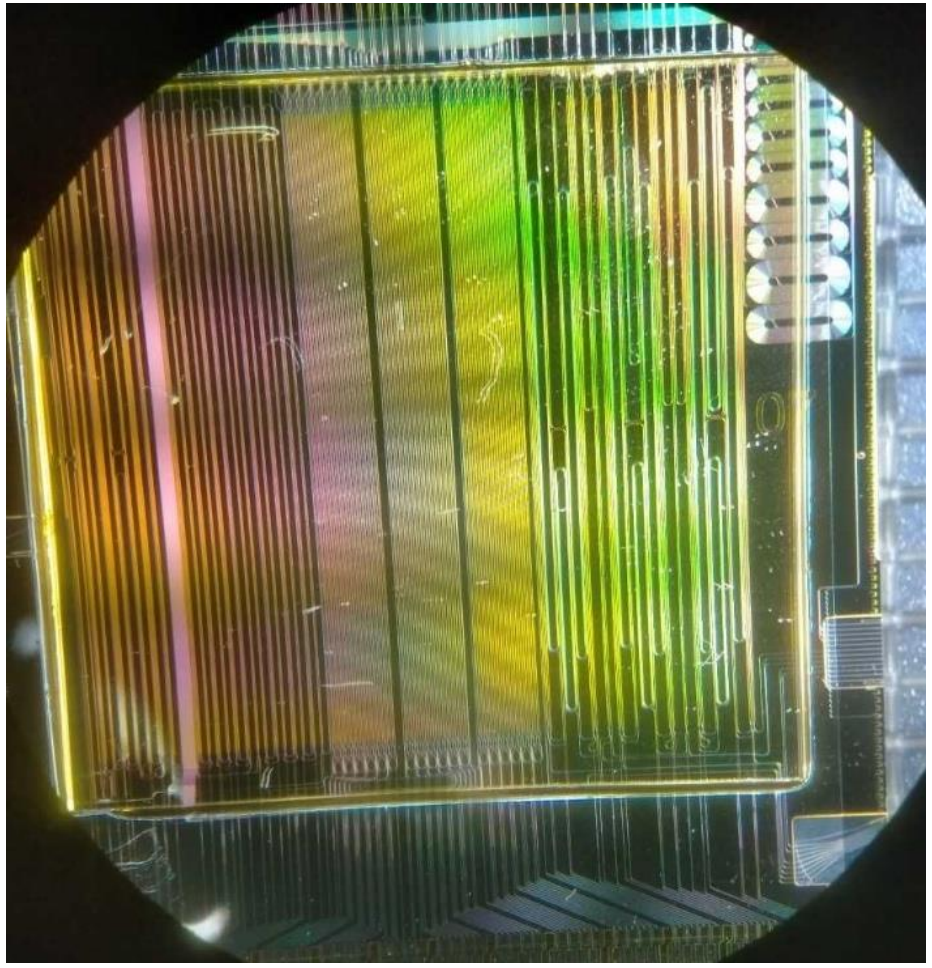
Chip Fabrication

TriPleX Size = 22 mm X 22.7 mm

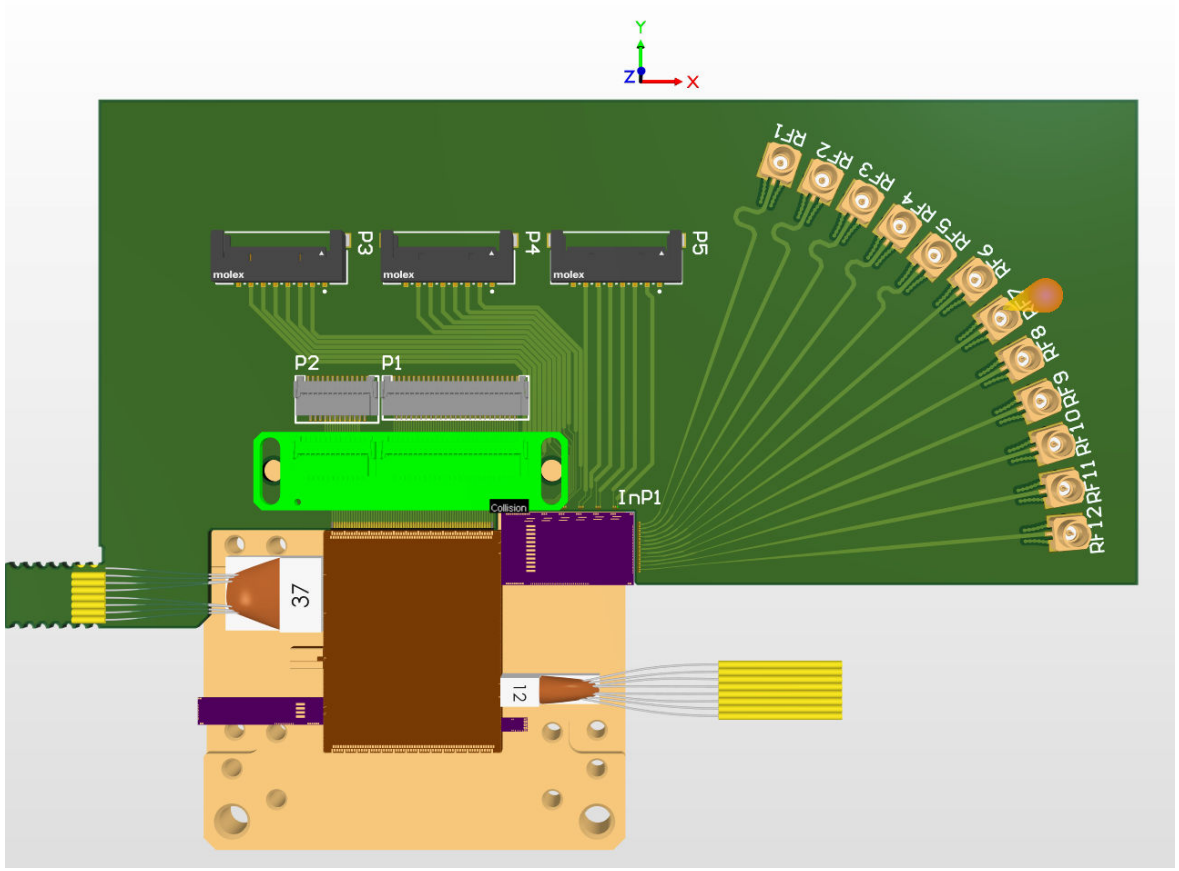
Fiber array
for monitoring
& characterization

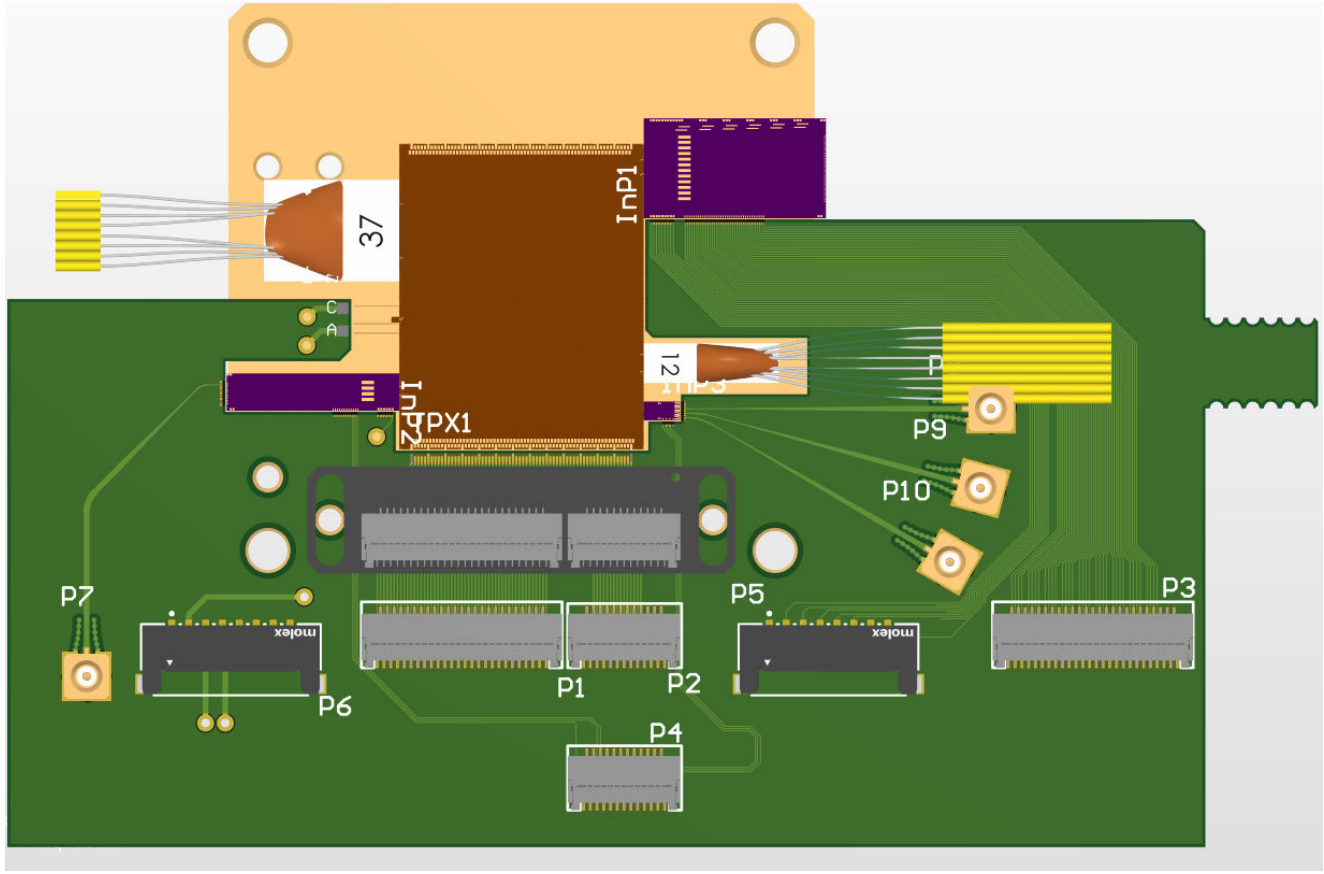


Fiber array
for monitoring
& characterization

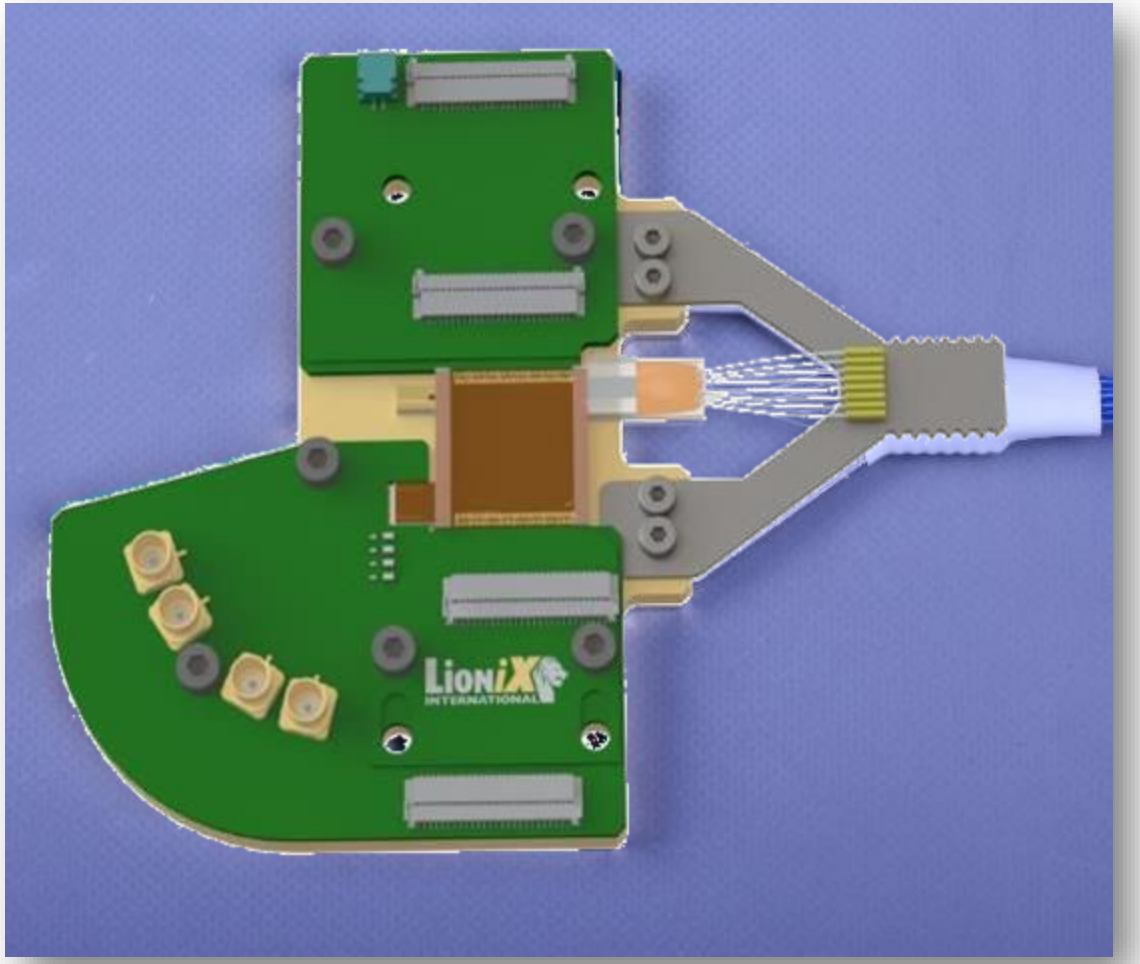


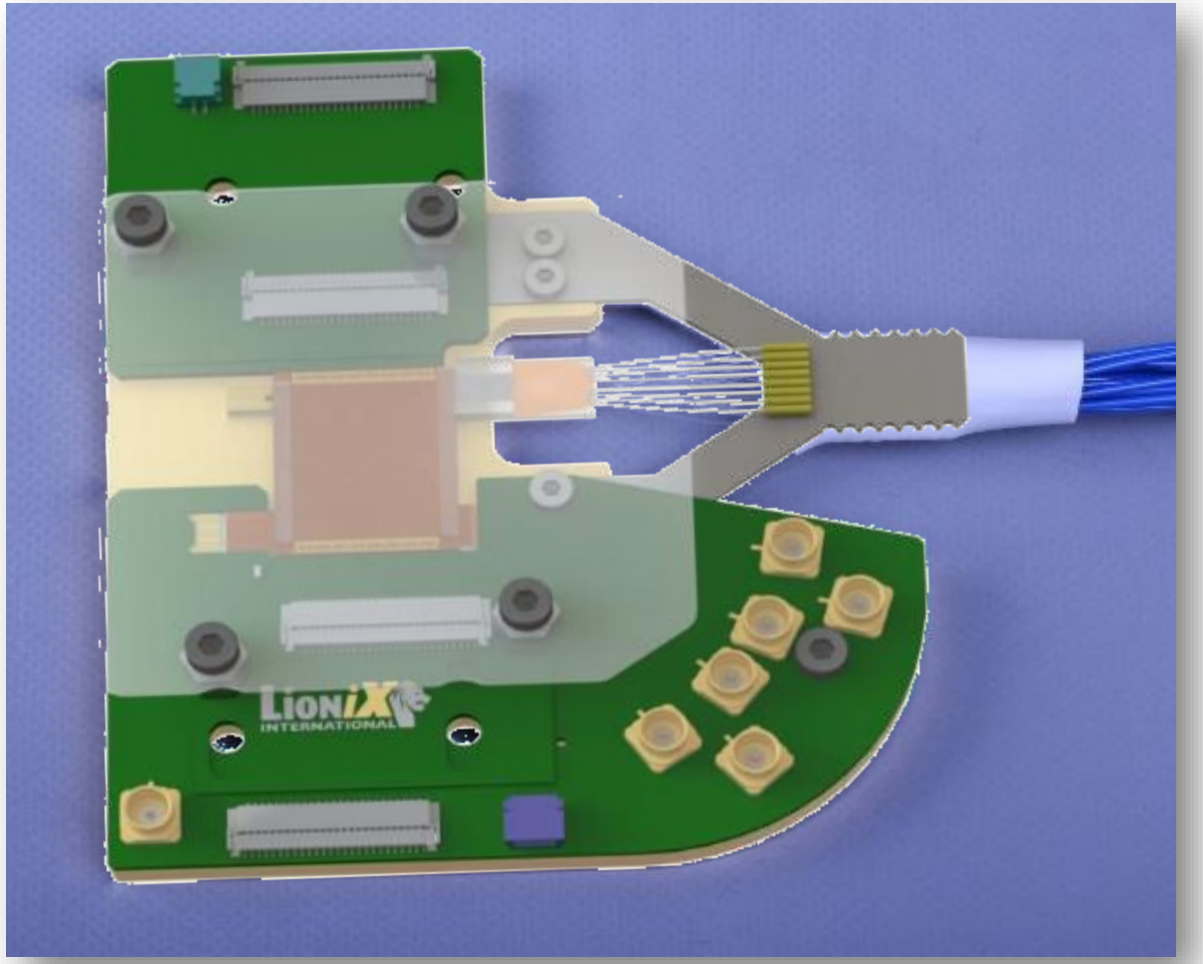
PCB Design


Y
Z
X
RF1
RF2
RF3
RF4
RF5
RF6
RF7
RF8
RF9
RF10
RF11
RF12
P3
P4
P5
molex
molex
molex
P2
P1
InP1
Collision
37
12

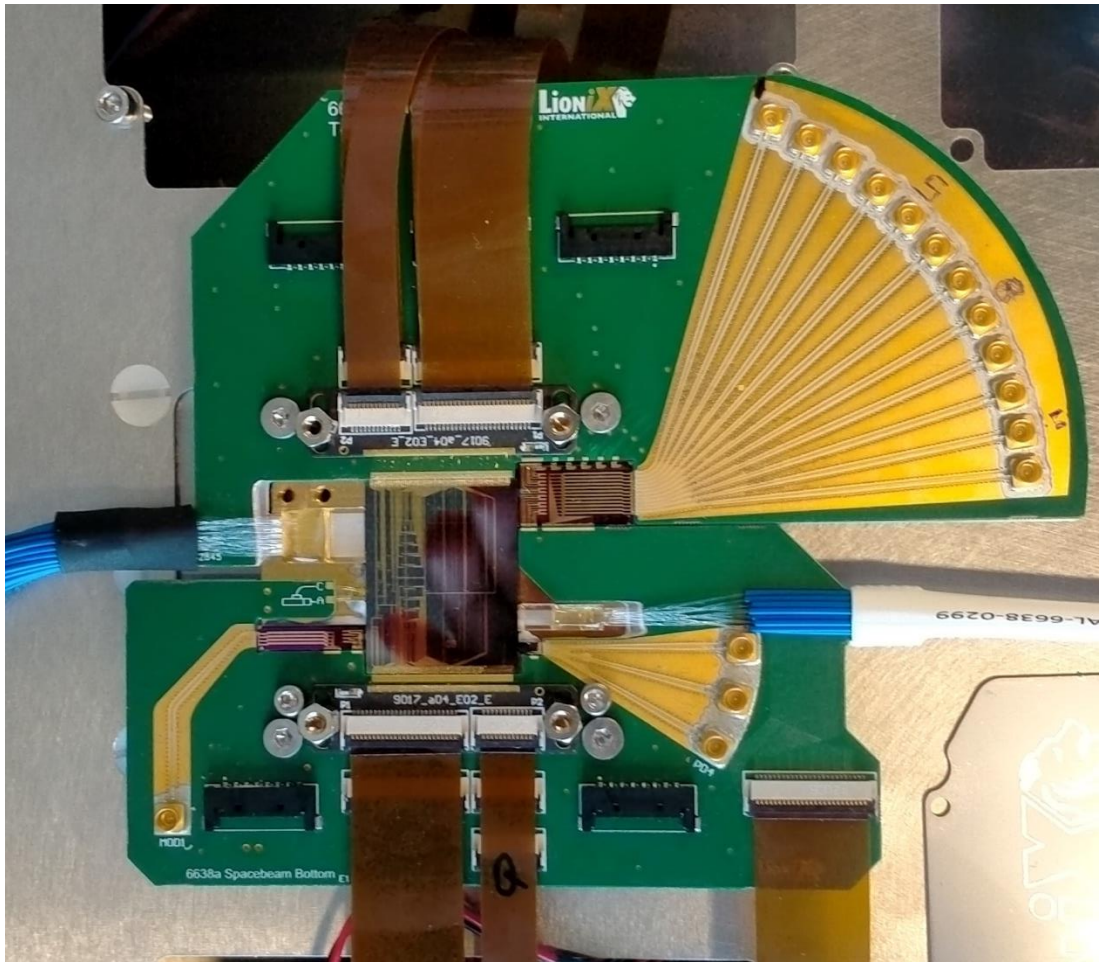

37
InP1
InP2
PX1
12
P9
P10
P7
P6
P1
P2
P4
P5
P3
molex
molex

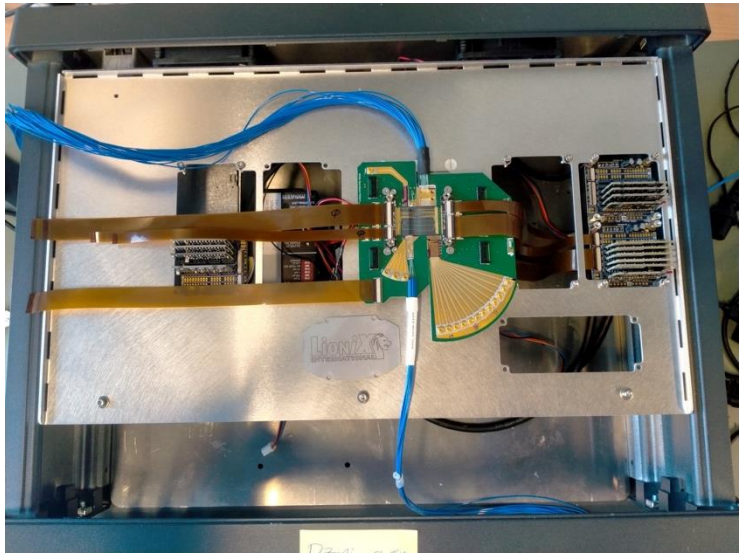
Precision Manufacturing



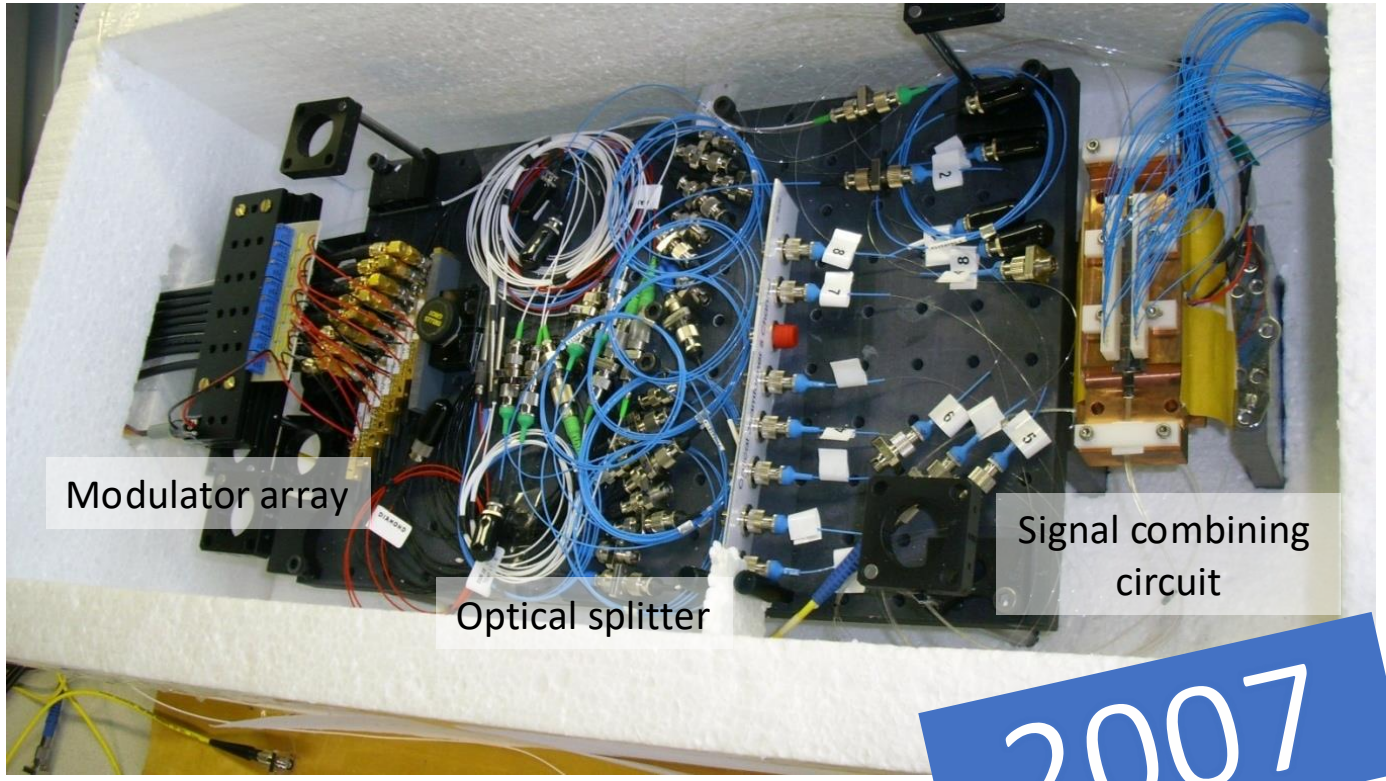


Driving Electronics for Characterisation

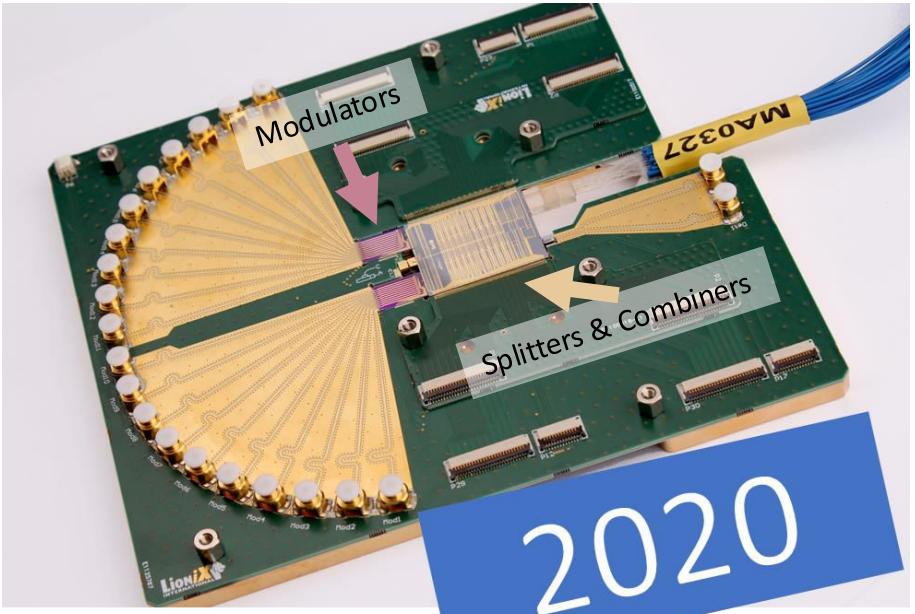




Progress



2007



2020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